

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

600V CoolMOS™ C7 Power Transistor
IPP60R180C7

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)} \cdot A$ below $10\text{Ohm} \cdot \text{mm}^2$.

Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Suitable for applications such as server, telecom and solar
- Higher switching frequencies possible without loss in efficiency due to low E_{oss} and Q_g

Applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

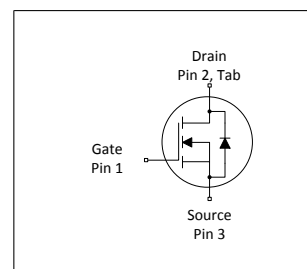
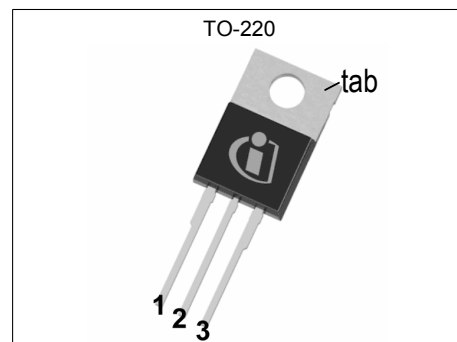


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	180	$m\Omega$
$Q_{g,typ}$	24	nC
$I_{D,pulse}$	45	A
$I_{D,continuous} @ T_j < 150^\circ\text{C}$	22	A
$E_{oss}@400\text{V}$	2.7	μJ
Body diode di/dt	350	$\text{A}/\mu\text{s}$

Type / Ordering Code	Package	Marking	Related Links
IPP60R180C7	PG-TO 220	60C7180	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	13 8	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	45	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	53	mJ	$I_D=3.3\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.26	mJ	$I_D=3.3\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	3.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	68	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	13	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	45	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	20	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 5.2\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	350	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 5.2\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.832	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.26mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.155 0.346	0.180 -	Ω	$V_{GS}=10V$, $I_D=5.3A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=5.3A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.85	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1080	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	18	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	34	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	349	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	9.3	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.3A$, $R_G=10\Omega$; see table 9
Rise time	t_r	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.3A$, $R_G=10\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.3A$, $R_G=10\Omega$; see table 9
Fall time	t_f	-	6	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.3A$, $R_G=10\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	$V_{DD}=400V$, $I_D=5.3A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	8	-	nC	$V_{DD}=400V$, $I_D=5.3A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	24	-	nC	$V_{DD}=400V$, $I_D=5.3A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400V$, $I_D=5.3A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=5.3A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	280	-	ns	$V_R=400V$, $I_F=5.3A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	2.6	-	μC	$V_R=400V$, $I_F=5.3A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	21	-	A	$V_R=400V$, $I_F=5.3A$, $di_F/dt=100A/\mu s$; see table 8

5 Electrical characteristics diagrams

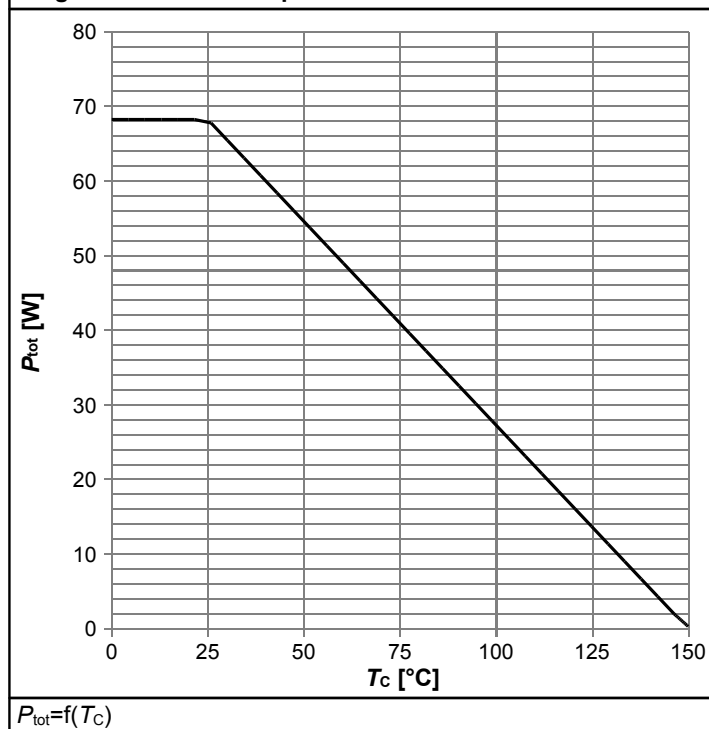
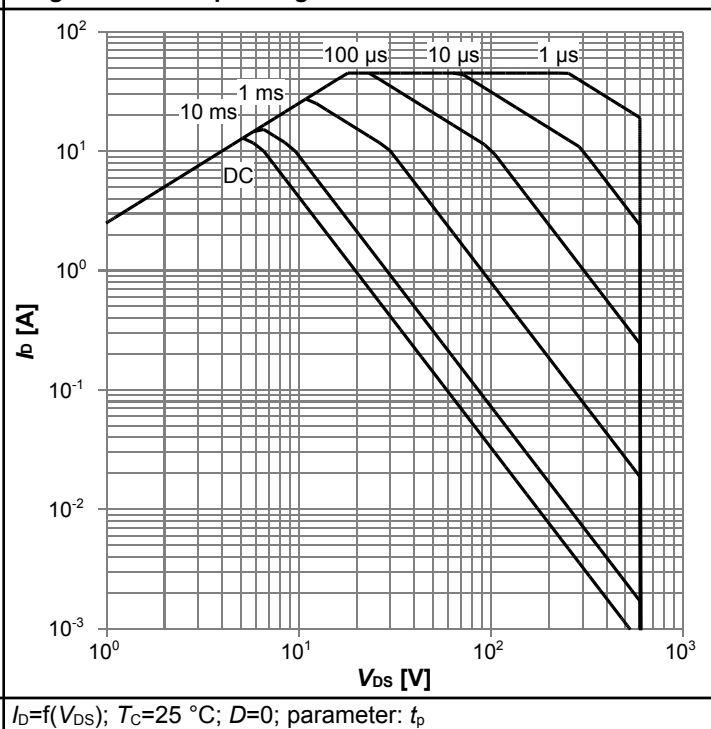
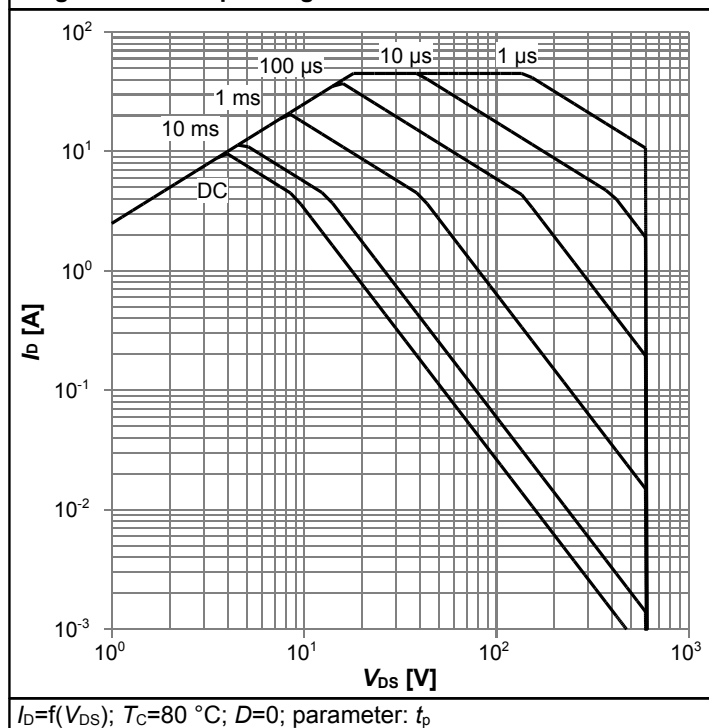
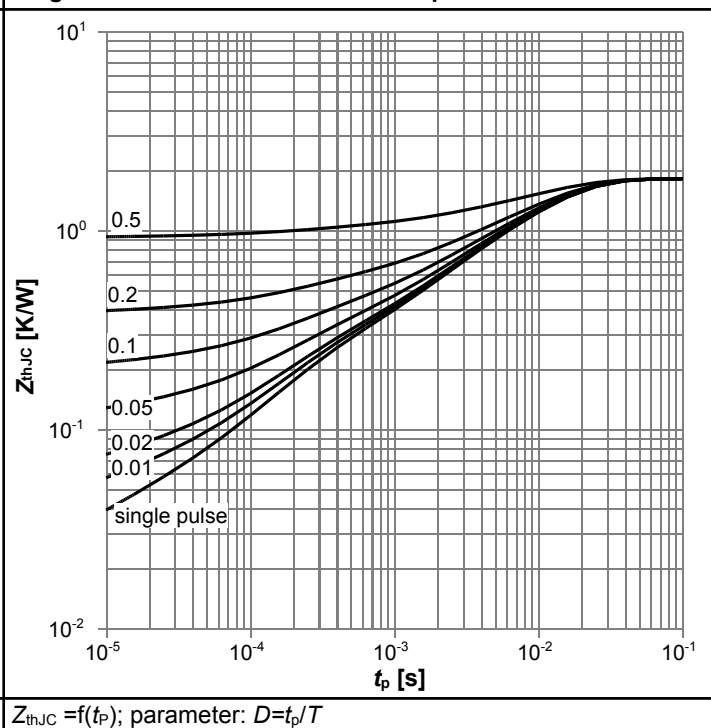
Diagram 1: Power dissipation

Diagram 2: Safe operating area

Diagram 3: Safe operating area

Diagram 4: Max. transient thermal impedance


Diagram 5: Typ. output characteristics

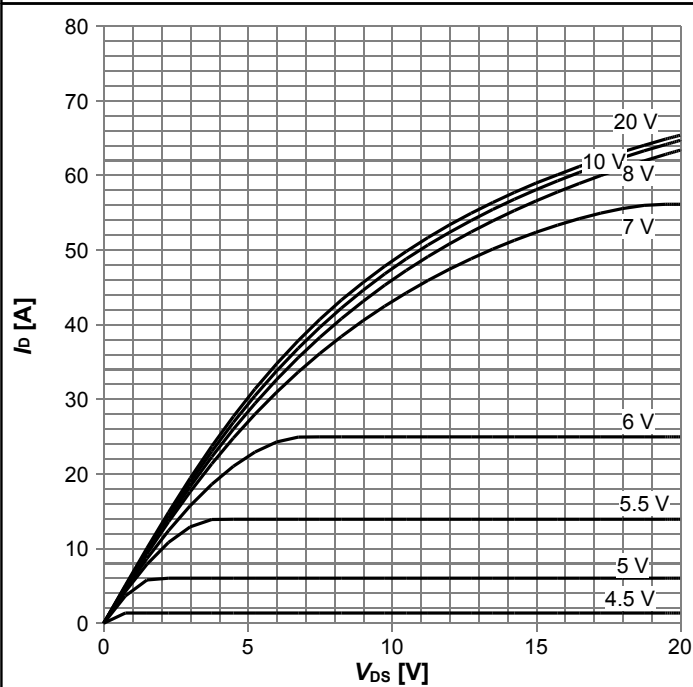

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics

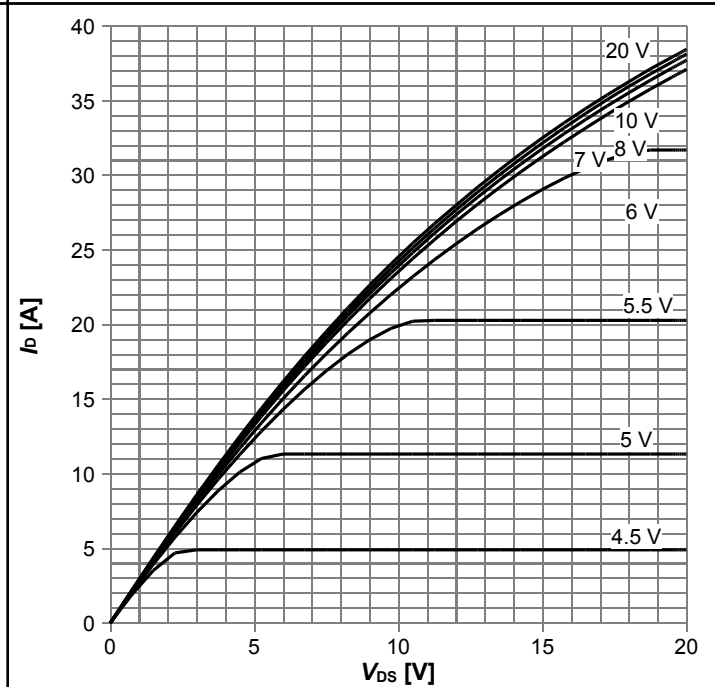

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

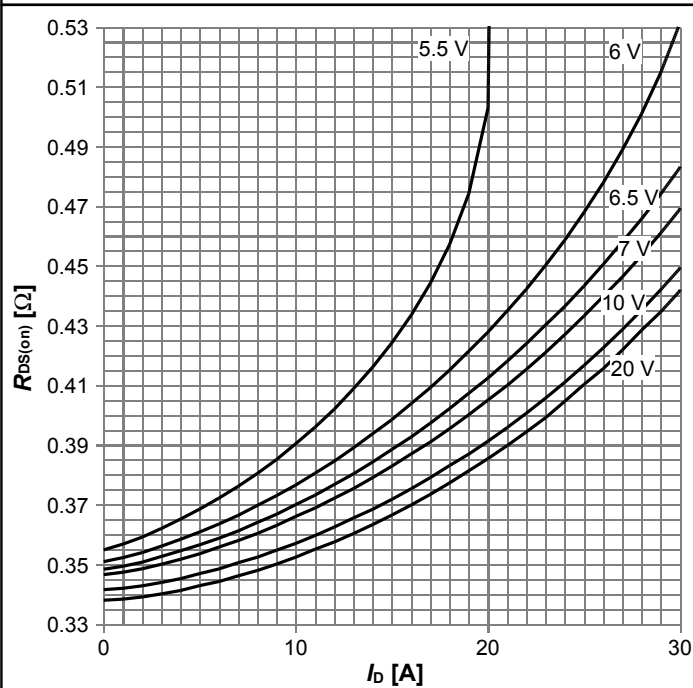

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

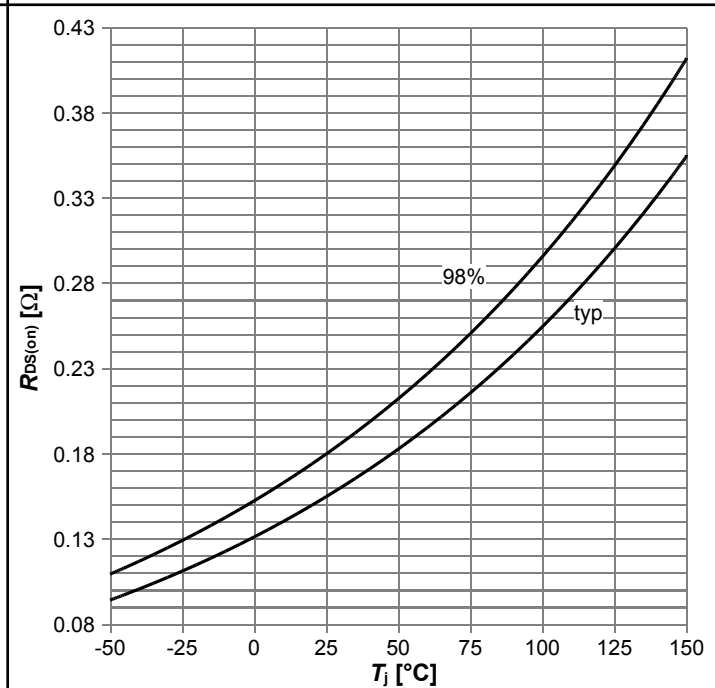

 $R_{DS(on)} = f(T_J); I_D = 5.3\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

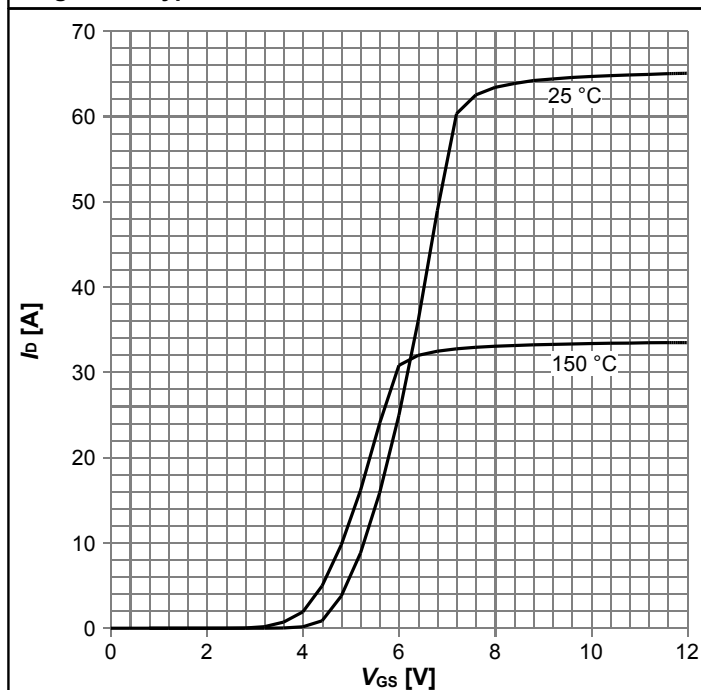

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

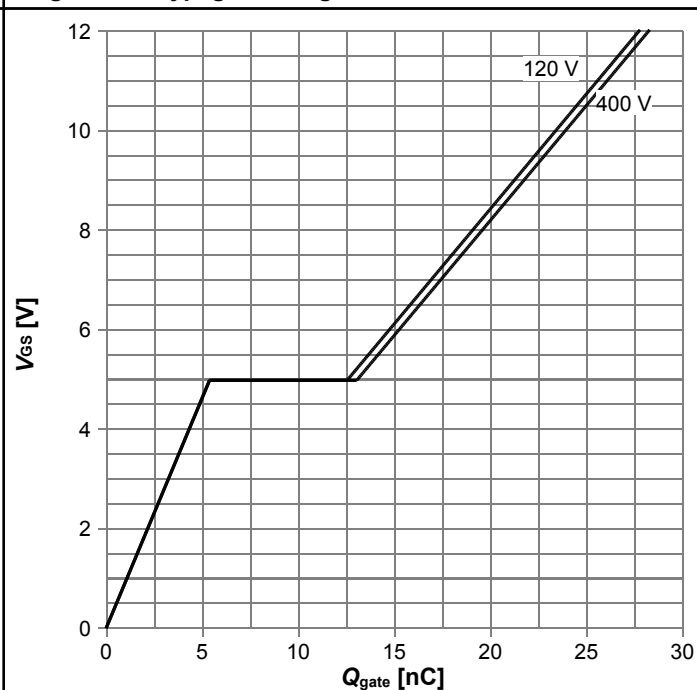

 $V_{GS} = f(Q_{gate}); I_D = 5.3 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

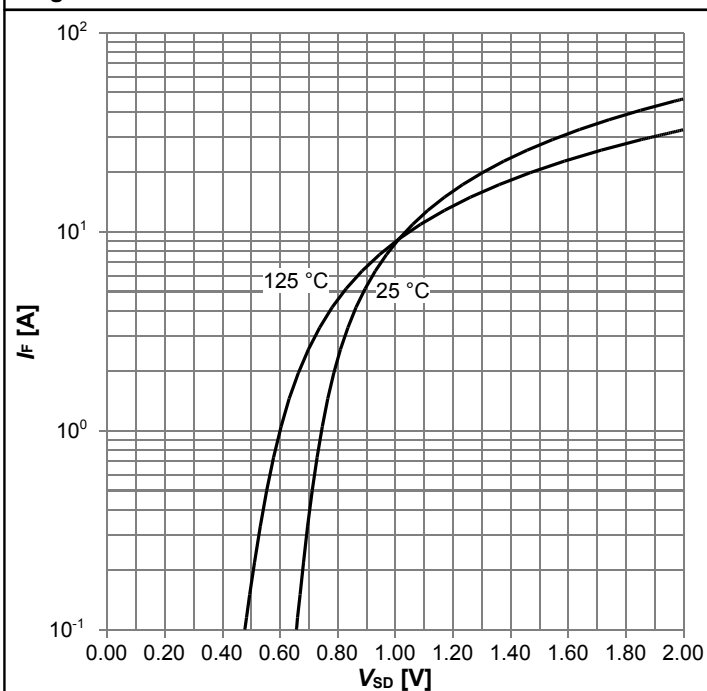

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

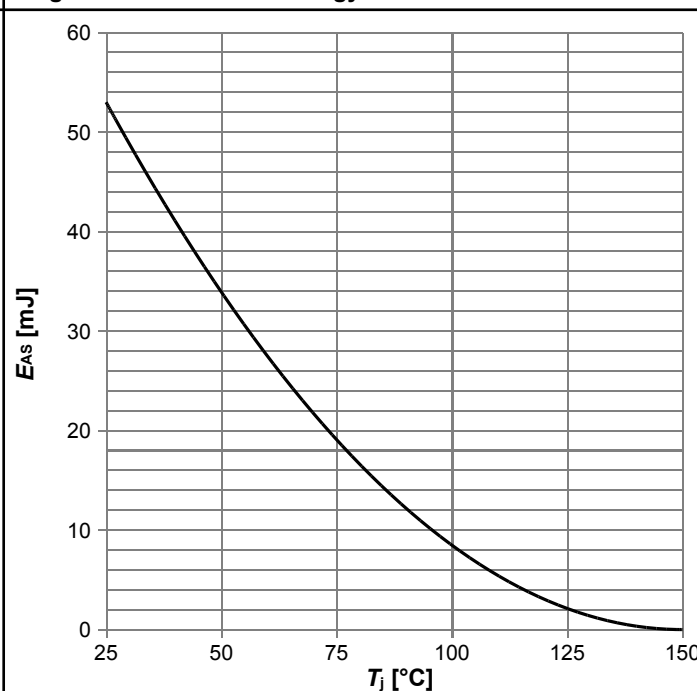
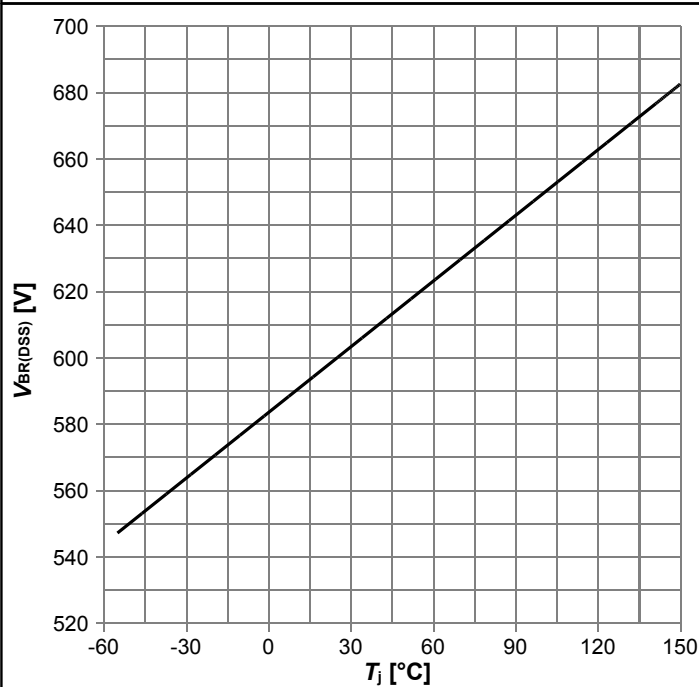
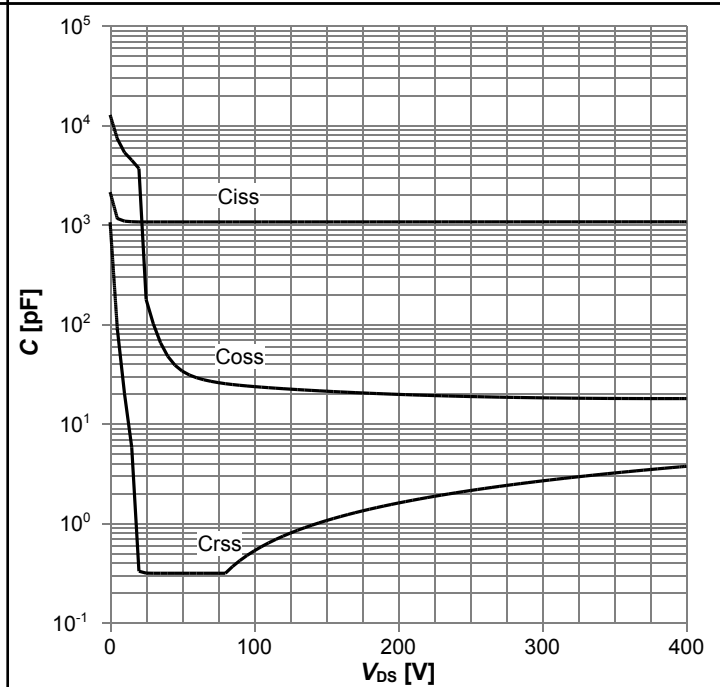

 $E_{AS} = f(T_j); I_D = 3.3 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



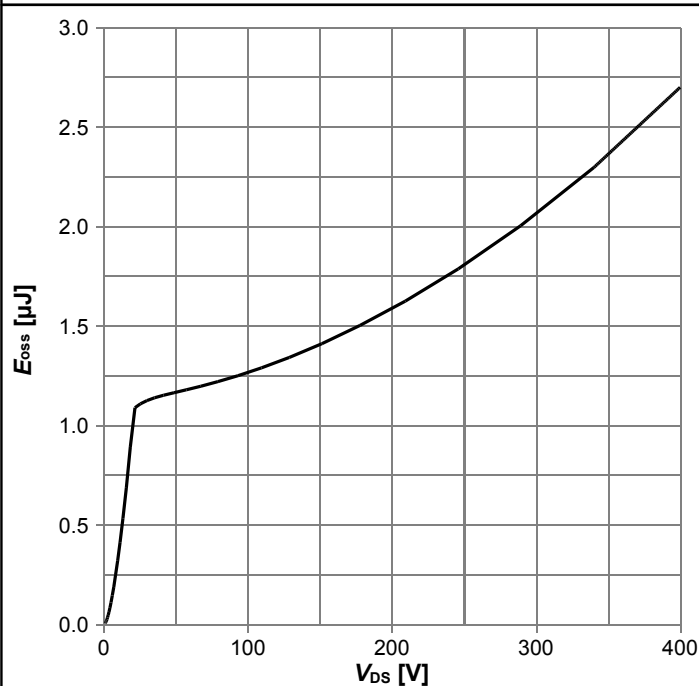
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics

$R_{g1} = R_{g2}$

Diode recovery waveform

Table 9 Switching times

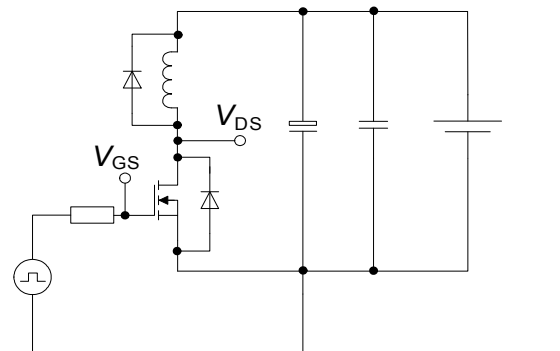
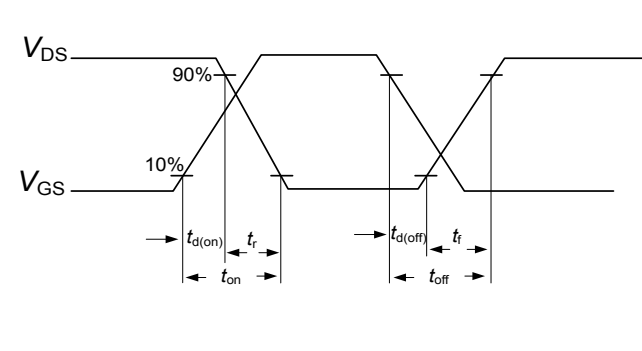
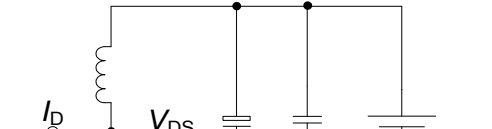
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a switching test setup for an inductive load. A MOSFET is driven by a pulse generator connected to its gate through a resistor. The drain of the MOSFET is connected to an inductor, which is in series with a load resistor and a parallel combination of a load capacitor and a freewheeling diode. The source of the MOSFET is grounded. The drain-source voltage is labeled V_{DS} and the gate-source voltage is labeled V_{GS}.	 The timing diagram shows the relationship between the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) during switching transitions. The diagram defines the following parameters: $t_{d(on)}$: Delay time from the 10% rise of V_{GS} to the 90% rise of V_{DS}. t_r: Rise time of V_{DS} from 90% to 100%. t_{on}: Total turn-on time from the 10% rise of V_{GS} to the steady-state high level of V_{DS}. $t_{d(off)}$: Delay time from the 90% fall of V_{DS} to the 10% fall of V_{GS}. t_f: Fall time of V_{DS} from 90% to 10%. t_{off}: Total turn-off time from the 90% fall of V_{DS} to the steady-state low level of V_{DS}.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

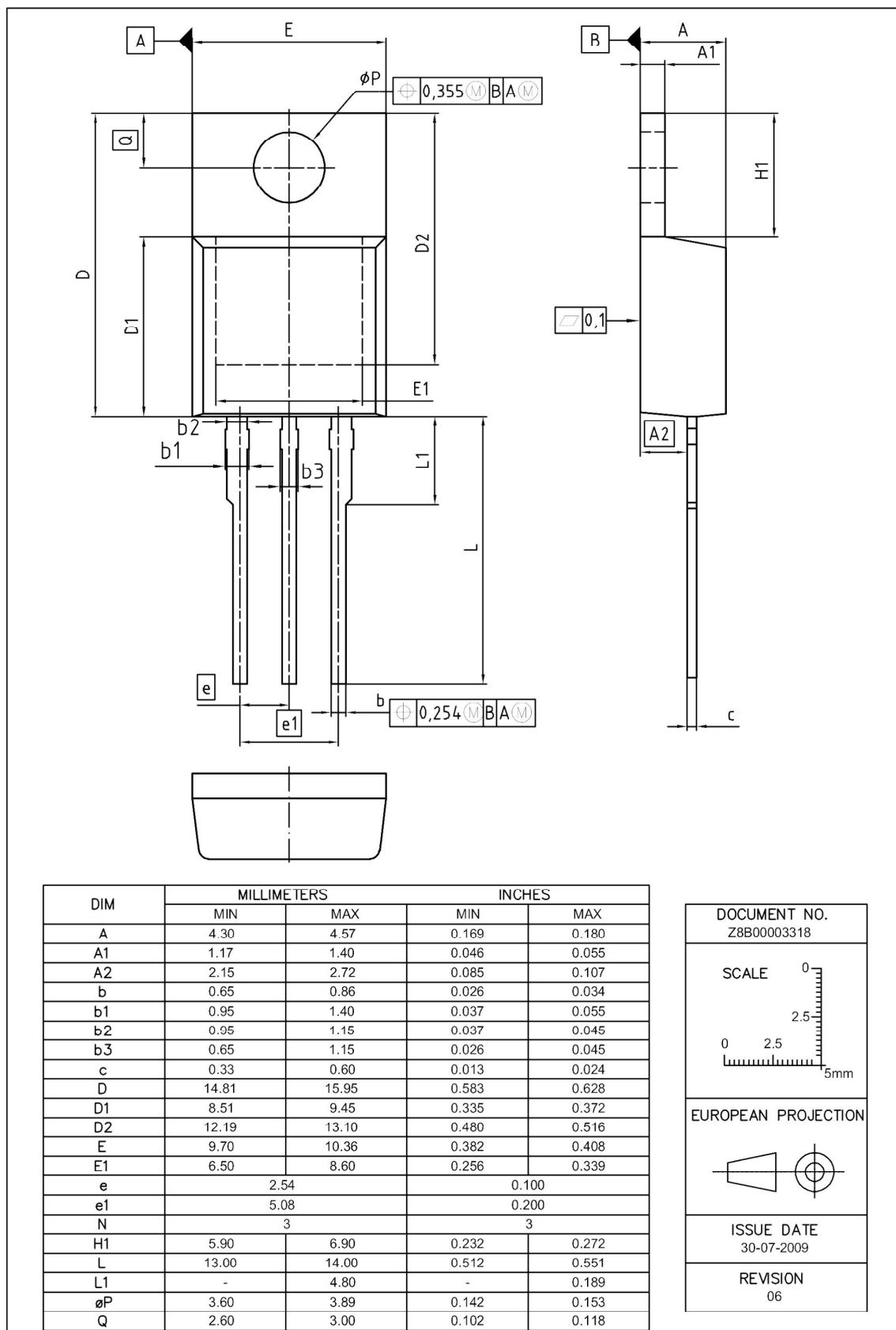


Figure 1 Outline PG-TO 220, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPP60R180C7

Revision: 2015-05-08, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-05-08	Release of final version

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